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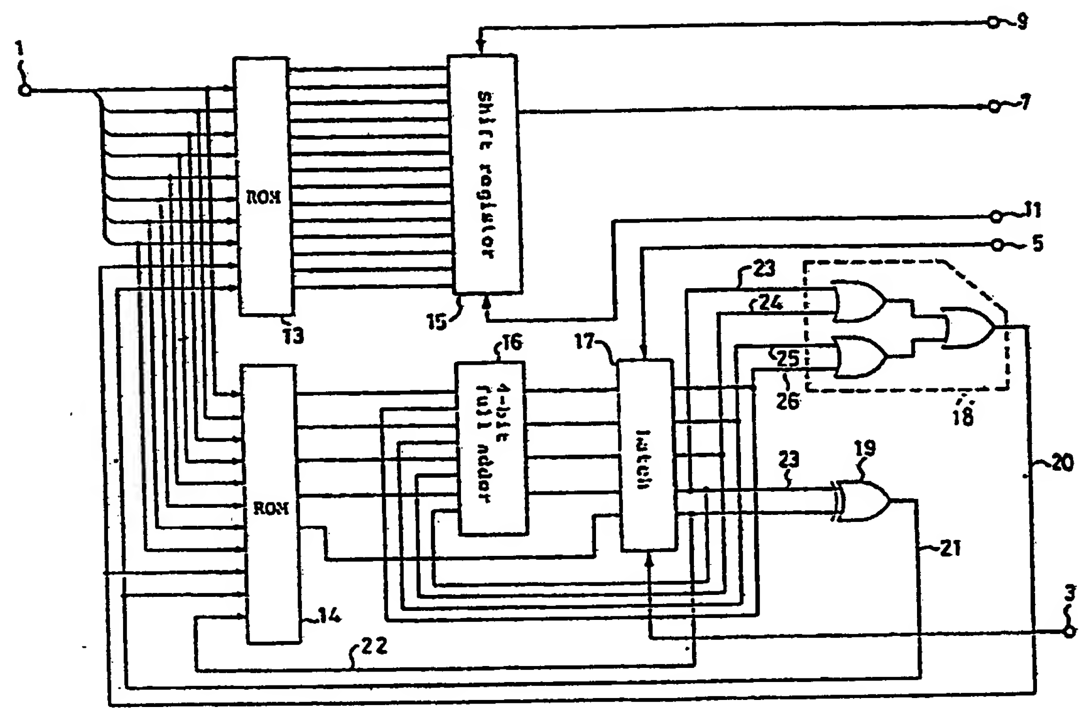
(54) **Digital data recording and reproducing method.**

(57) In a digital data recording and reproducing method, a digital data sequence is divided into every 8-bit digital data, when the divided 8-bit digital data is encoded to 14-bit code, an 8-bit digital data wherein value of DSV is limited in a predetermined range is selected from two codes corresponding to 8-bit digital data, and in an encoding process, the number of bit "0" which is inserted between two bits "1" in the code sequence is restricted to a number of from one to eight, and hence, DC component in the code sequence is eliminated.

$m = 8$
$n = 14$
DSV is limited

$d, k = 1, 8$

FIG.1



1
9
7
11
5
ROM
Shift register
13
15
16
4-bit full adder
17
latch
23
24
25
26
18
19
23
20
21
ROM
14
22
3

TITLE OF THE INVENTION

Digital data recording and reproducing method

FIELD OF THE INVENTION AND RELATED ART STATEMENT

1. FIELD OF THE INVENTION

The present invention relates generally to a digital data processing method, and more particularly to a new and improved method for encoding, reproducing binary digital data and for recording synchronizing signal thereof.

2. DESCRIPTION OF THE RELATED ART

When digital data are recorded on a magnetic tape or are reproduced therefrom by using a rotary magnetic head, encoded binary signals corresponding to the digital data are generally transmitted to the rotary magnetic head through a rotary transformer. If the encoded binary signals contain DC component, these are not normally recorded on the magnetic tape since the rotary transformer does not transmit the DC component.

A prior art for eliminating the DC component of the encoded binary signals is shown in the U.S. Patent 4,216,460. In this patent, the 8-bit word is transformed into the 10-bit code word. However, density ratio is smaller than 1.
(Density ratio = Tmin/T, where, T is data clock and Tmin is minimum magnetization reversal interval)

In other prior art, the U.S. Patent 4,323,931, the three position modulation method which is a high density modulation method, is disclosed. Density ratio of this method is greater than 1, but, DC component in the encoded binary signal is not eliminated.

In the conventional digital data recording method, digital data sequence is divided into predetermined data units. A frame synchronizing signal and an error detection code are added to an each data unit, thereby to form a frame. The frame with the frame synchronizing signal and the error detecting code are encoded and are recorded on a recording medium. In the reproducing process, the frame synchronizing signal is detected from the reproduced code sequence. The detected frame synchronizing signals are used for synchronization of clock signals, and for control of starting point, whereby the respective unit of the digital data are distinguished with each other. As mentioned above, since the frame synchronizing signal has the important function, it must be surely detected. As to selection of a method from many kinds of the frame synchronizing signals in the conventional methods, in order to avoid misdetection of the frame synchronizing signal when the position of a bit is shifted to an abnormal position, a special bit

sequence, for example, the bit sequence with a long magnetization reversal interval which is used. frequently is adopted. However, the plural bit requence, exist in the code sequence and there is a fear of misdetection of the frame synchronizing signals. In order to avoid the above-mentioned misdetection, a protection circuit for synchronizing signal which utilizes cyclic issue of the frame synchronizing signal is necessary. Nevertheless, there is a defect that when the frame synchronizing signals of continuous data units are not detected due to dropout of the recording medium, comparatively long time is required for resumption of the certain detection of the frame synchronizing signals. Therefore, it is required to select the most suitable protection circuit system for synchronizing signal in accordance with the function of the recording and reproducing apparatus. These circuits are generally formed by complex circuits, hence a careful design of the system is required.

OBJECT AND SUMMARY OF THE INVENTION

An object of the present invention is to provide a high density and a great DR digital encoding method for magnetic recording wherein DC component of a code sequence is little and a minimum magnetization reversal interval is large.

Another object of the present invention is to provide a digital encoding method wherein a digital data sequence is cut at every predetermined sections of digital data, and a frame synchronizing signal and an error detecting code are added to every digital data units. As a result, when the digital data are reproduced, misdetection of the frame synchronizing signal decreases. In this specification, the high level and the low level of the encoded signal are shown by representations of "1" and "0", respectively.

In order to realize the first object, the digital data sequence is divided into 8-bit digital data, and every 8-bit digital data are encoded to 14-bit codes, wherein when these 8-bit digital data are encoded, number of bits of value "0" which are inserted between two bits of value "1" are restricted to eight and below.

In order to realize the second object,

said 8-bit digital data are encoded to a 14-bit code sequence, an optionally selected successive 16-bit code is taken out from the 14-bit code sequence, and the 16-bit code is made to does not coincide to an N bit code sequence ($N \geq 16$) including a bit sequence "1000000010000000". The N bit code sequence is recorded as a frame synchronizing signal on a recording medium.

Digital data recording and reproducing method in accordance with the present invention comprises:

dividing digital data to every 8-bit digital data,

selecting one of two codes wherein an absolute value of digital sum variation of NRZI coded wave form wherein a code sequence of the digital data is encoded to NRZI code decreases,

wherein number of bit "0" inserted between two bits "1" in a code sequence is restricted to a number from one to eight and below, when the 8-bit digital data is allotted to one or two codes, and

digital data recording and reproducing apparatus comprises:

means for producing NRZI coding of a code sequence wherein an 8-bit digital data is sequentially coded,

means for issuing a control signal which selects 14-bit code wherein an absolute value of digital sum variation of a wave form of the NRZI code decreases, and

means for issuing a 14-bit code corresponding to the 8-bit digital data by input of the control signal.

BRIEF DESCRIPTION OF THE DRAWING

FIG.1 is a circuit diagram of an encoder for use in the digital data recording and reproducing method in accordance with the present invention.

FIG.2 is a timing chart showing change of polarity in a digital code sequence and change of DSV (digital sum variation) in a code sequence wherein eight bit digital data are encoded to 14-bit code, in an embodiment of the present invention.

FIG.3 is a timing chart showing an operation of the encoder in the embodiment in accordance with the present invention.

FIG.4 is a circuit diagram of a decoder in the embodiment.

FIG.5 is a timing chart showing an operation of the decoder.

FIG.6(a) is a block diagram of an encoding and a recording circuits in the embodiment.

FIG.6(b) is a block diagram of a decoding and reproducing circuit in the embodiment.

FIG.7 is a frame construction in the embodiment in accordance with the present invention.

FIG.8 is a circuit diagram of the circuit for adding the frame synchronizing signal of the embodiment.

FIG.9 is a timing chart showing an operation of the circuit for adding the frame synchronizing

signal.

FIG.10 is a circuit diagram of the detecting circuit of the embodiment.

FIG.11(a) and FIG.11(b) are timing charts showing an operation of CDS (code word digital sum) in the embodiment.

FIG.12(a), FIG.12(b) and FIG.12(c) are timing charts showing a relation between CDS and DSV of the embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An encoding method in accordance with the present invention relates to convert an 8-bit digital data to 14-bit code. As well known, 14-bit binary code can represent sixteen thousand three hundred and eighty-four data. Four hundred and seven code patterns of 8-bit digital data are selected from the sixteen thousand three hundred and eighty-four data according to the following algorithm. A truth tables of codes are shown in Table 1.

Table 1

Data	Group A Code	C D S	Group B Code	C D S
00	01001010101010	0	01001010101010	0
01	01010100101010	0	01010100101010	0
02	01010101010010	0	01010101010010	0
03	10010010101010	0	10010010101010	0
04	10010101001010	0	10010101001010	0
05	10010101010100	0	10010101010100	0
06	10100100101010	0	10100100101010	0
07	10100101010010	0	10100101010010	0
08	10101001001010	0	10101001001010	0
09	10101001010100	0	10101001010100	0
0A	10101010010010	0	10101010010010	0
0B	10101010100100	0	10101010100100	0
0C	01001001010010	0	01001001010010	0
0D	01010010010010	0	01010010010010	0
0E	01010010100100	0	01010010100100	0
0F	01001001000100	0	01001001000100	0
10	10001000100100	0	10001000100100	0
11	10001001001000	0	10001001001000	0
12	10010001000100	0	10010001000100	0
13	10010010001000	0	10010010001000	0
14	01001000101010	0	01001000101010	0
15	01001010100010	0	01001010100010	0

16	01010001001010	0	01010001001010	0
17	01010001010100	0	01010001010100	0
18	01010100100010	0	01010100100010	0
19	01010101000100	0	01010101000100	0
1A	10010001010010	0	10010001010010	0
1B	10010010100010	0	10010010100010	0
1C	10100010010010	0	10100010010010	0
1D	10100010100100	0	10100010100100	0
1E	10100100100010	0	10100100100010	0
1F	10100101000100	0	10100101000100	0
20	01000100010010	0	01000100010010	0
21	01000100100100	0	01000100100100	0
22	01000101001000	0	01000101001000	0
23	01001000100010	0	01001000100010	0
24	01001010001000	0	01001010001000	0
25	01010010000100	0	01010010000100	0
26	10000100010100	0	10000100010100	0
27	10000100101000	0	10000100101000	0
28	10001000010010	0	10001000010010	0
29	10001010010000	0	10001010010000	0
2A	10010000100010	0	10010000100010	0
2B	10010100010000	0	10010100010000	0
2C	10100010000100	0	10100010000100	0
2D	10100100001000	0	10100100001000	0
2E	10010000101010	0	10010000101010	0

Data	Group A		Group B	
	Code	C D S	Code	C D S
2F	10010101000010	0	10010101000010	0
30	10100001001010	0	10100001001010	0
31	10100001010100	0	10100001010100	0
32	10101001000010	0	10101001000010	0
33	10101010000100	0	10101010000100	0
34	01000010001010	0	01000010001010	0
35	01000010010100	0	01000010010100	0
36	01000010101000	0	01000010101000	0
37	01010001000010	0	01010001000010	0
38	01010100001000	0	01010100001000	0
39	10000100001010	0	10000100001010	0
3A	10000101010000	0	10000101010000	0
3B	10100001000010	0	10100001000010	0
3C	10101000010000	0	10101000010000	0
3D	01000100000100	0	01000100000100	0
3E	01001000001000	0	01001000001000	0
3F	01000010000010	0	01000010000010	0
40	01010000010000	0	01010000010000	0
41	10001000000100	0	10001000000100	0
42	10010000001000	0	10010000001000	0
43	10000100000010	0	10000100000010	0
44	10100000010000	0	10100000010000	0

45	01001001010100	2	00010100100100	-4
46	01001010100100	2	00100100010100	-4
47	01010100100100	2	00101000100100	-4
48	10001001010010	2	01001000101000	-4
49	10010010010010	2	01010010010000	-4
4A	00010101010010	-2	10000100100010	4
4B	00101010100010	-2	00100010010000	4
4C	01010010100010	-2	10000010000100	4
4D	00001000101010	-2	01010100001010	4
4E	00010001010100	-2	10000101010010	4
4F	00010101000100	-2	10100101010000	4
50	10100100010010	2	00001010010010	-4
51	10100101001000	2	00100100001010	-4
52	10000100010010	2	00101000010010	-4
53	00010001001000	2	01001001010000	-4
54	00100100010000	2	10010000101000	-4
55	10101000101010	2	10100001001000	-4
56	00101000100010	-2	01000101000010	4
57	01000100010100	-2	10000101000100	4
58	01001000010010	-2	10001010000100	4
59	00100010101010	2	00001010000100	-4
5A	01010001000100	-2	00010001010000	4
5B	10001000101000	-2	01000010001000	4
5C	00101010001010	2	01001000001010	-4
5D	01000100101010	2	10010000010100	-4

Data	Group A Code	Group A CDS	Group B Code	Group B CDS
5E	10010010010000	-2	01000001010010	4
5F	00001000100010	-2	10000001001010	4
60	00010010000100	-2	10010010000010	4
61	01010010001010	2	00010010000010	-4
62	00010000010000	-2	00010000010100	4
63	01010000101010	-2	01000001000100	4
64	01010100010010	2	10010000001010	-4
65	10001010100010	2	00100100000010	-4
66	10010100100010	2	01001000000010	-4
67	10100010001010	2	10010000000010	-4
68	10100010101000	2	00010100010100	-6
69	10101010001000	2	00101000101000	-6
6A	10100101000010	-2	10001010001010	6
6B	01000100100010	2	00001010010100	-6
6C	10000010001010	2	00010100001010	-6
6D	10001000100010	2	00101000010100	-6
6E	10010010000100	2	01010000101000	-6
6F	00010000100100	2	10100001010000	-6
70	01000100001010	-2	10001010101000	6
71	01010000100010	-2	10010100101000	6
72	10001001010000	-2	10000010001000	6
73	10100001000100	-2	10000101010100	6

74	00010001000010	-2	10010101010000	6
75	00100100000100	-2	10101001010000	6
76	10101010000010	-2	00100001010000	6
77	00100001000100	2	01010000010100	-6
78	10001000001010	-2	01000010010000	6
79	01001000010000	2	00001010000010	-6
7A	00101000001000	-2	10101000001010	6
7B	10001000001000	2	01010000001010	-6
7C	00100101000010	2	00010100000010	-6
7D	01010000001000	-2	00100000101000	6
7E	01000010010010	2	10100000001010	-6
7F	10001000000010	-2	10000000100010	6
80	01001001000010	2	01010000000010	-6
81	01000010100100	2	00101000000010	-6
82	10010000000100	-2	01000001001000	6
83	01000100000010	-2	10001010000010	6
84	00100001010010	2	10100000010100	-6
85	01001000000100	-2	10000010100010	6
86	00100010000010	-2	10000010101010	6
87	10100000100010	-2	10000001000100	6
88	01000100001000	2	10100000101000	-6
89	00010010010000	2	00101000001010	-6
8A	10100000101010	-2	10000101000010	6
8B	00010100001000	-2	10101000010100	6
8C	00001010001000	-2	10010100001010	6
8D	10010000010010	-2	10000101001010	6

Data	Group A		Group B	
	Code	C D S	Code	C D S
8E	10001000010100	-2	10101000101000	6
8F	01000101010000	-2	10010100010100	6
90	00001010100010	-2	10001010010100	6
91	00001000101000	2	01010001010000	-6
92	10001010001000	2	00101001010000	-6
93	10000100100100	2	00010101010000	-6
94	01000101000100	2	00001010101000	-6
95	00100010100010	2	00001010001010	-6
96	10100001010010	-2	10000100010000	6
97	10101000100010	2	00010100101000	-6
98	10100010010100	2	10100000000100	-4
99	10010101000100	2	01010000000100	-4
9A	10010001010100	2	00101000000100	-4
9B	10001000101010	2	10100000010010	-4
9C	01010101000010	-2	10000000010000	4
9D	00001010101010	-2	00100000010010	4
9E	01010010101000	2	00010100000100	-4
9F	00001000001000	-2	10010100000100	4
A0	00001001000100	-2	10000010100100	4
A1	10100010001000	-2	01001010000010	4
A2	01000101010010	2	10100000100100	-4
A3	00101010101000	2	01010000010010	-4

A4	10010000100100	-2	10000001000010	4
A5	01010100010000	-2	00100000100100	4
A6	01001010010000	-2	00010000101000	4
A7	10101010100010	2	00001001000010	-4
A8	01000100101000	-2	10001001000010	4
A9	00101010001000	-2	10000010010010	4
AA	00100010101000	-2	01000010100010	4
AB	10001010101010	2	10010001010000	-4
AC	00100010001000	2	01010000100100	-4
AD	10001001000100	2	01001000010100	-4
AE	10101001000100	2	00100101010000	-4
AF	10100100100100	2	00001010100100	-4
B0	00100010001010	-2	10101000010010	4
B1	00010100100010	-2	10100100001010	4
B2	00001001010010	-2	01010101010000	4
B3	10100010100010	-2	01000010101010	4
B4	01010001010010	-2	01000100010000	4
B5	00101000101010	-2	00100001001000	4
B6	10010010100100	2	10100010010000	-4
B7	10010001001010	2	01010001001000	-4
B8	01010101001000	2	00101010010000	-4
B9	01010010010100	2	00100100101000	-4
BA	01001010010010	2	00010101001000	-4
BB	01001001001010	2	00010100010010	-4
BC	00101010010100	2	00010010101000	-4
BD	00100101010100	2	00010010001010	-4

Data	Group A		Group B	
	Code	CDS	Code	CDS
BE	00100101001010	2	00001001010100	-4
BF	10101001010010	2	00001001001010	-4
C0	00010100101010	-2	10101010010000	4
C1	10101010101000	-2	10101000100100	4
C2	10101010001010	-2	10100100101000	4
C3	10100010101010	-2	10100100010100	4
C4	10100100010000	-2	10010100010010	4
C5	10010001001000	-2	10010010101000	4
C6	01010010001000	-2	10010010001010	4
C7	01001001001000	-2	10001010100100	4
C8	01001000100100	-2	10001010010010	4
C9	00101001000100	-2	10000100101010	4
CA	00100101001000	-2	01010100101000	4
CB	00100100010010	-2	01010100010100	4
CC	00100010010100	-2	01001010101000	4
CD	00010010100100	-2	01001010001010	4
CE	00010010010010	-2	01000101010100	4
CF	00010001001010	-2	01000101001010	4
D0	00101001010010	-2	10001000010000	4
D1	10101010010100	-2	10000100001000	4
D2	10010101010010	2	00101001001000	-4
D3	10010100101010	2	00010010010100	-4

D4	10100101010100	-2	10101001001000	4
D5	10100101001010	-2	10010101001000	4
D6	01010101010100	-2	10010100100100	4
D7	01010101001010	-2	10010010010100	4
D8	01010010101010	-2	10001001010100	4
D9	00101010101010	-2	10001001001010	4
DA	00100100100100	-2	01001010010100	4
DB	10101010101010	2	00001000010000	-4
DC	00100000010000	0	00100000010000	0
DD	00001000000100	0	00001000000100	0
DE	00010000001000	0	00010000001000	0
DF	00101000010000	0	00101000010000	0
E0	00100001000010	0	00100001000010	0
E1	00001010010000	0	00001010010000	0
E2	00101010000100	0	00101010000100	0
E3	00101001000010	0	00101001000010	0
E4	00100001010100	0	00100001010100	0
E5	00010101000010	0	00010101000010	0
E6	00010000101010	0	00010000101010	0
E7	00100100001000	0	00100100001000	0
E8	00100010000100	0	00100010000100	0
E9	00010100010000	0	00010100010000	0
EA	00010000100010	0	00010000100010	0
EB	00001001001000	0	00001001001000	0
EC	00001000010010	0	00001000010010	0
ED	00100101000100	0	00100101000100	0

Data	Group A		Group B	
	Code	CDS	Code	CDS
EE	00100100100010	0	00100100100010	0
EF	00100010100100	0	00100010100100	0
F0	00100001001010	0	00100001001010	0
F1	00010010100010	0	00010010100010	0
F2	00010001010010	0	00010001010010	0
F3	00010101010100	0	00010101010100	0
F4	00010101001010	0	00010101001010	0
F5	00010010001000	0	00010010001000	0
F6	00010001000100	0	00010001000100	0
F7	00001000100100	0	00001000100100	0
F8	00100010010010	0	00100010010010	0
F9	00101010100100	0	00101010100100	0
FA	00101010010010	0	00101010010010	0
FB	00101001010100	0	00101001010100	0
FC	00101001001010	0	00101001001010	0
FD	00100101010010	0	00100101010010	0
FE	00100100101010	0	00100100101010	0
FF	00010010101010	0	00010010101010	0

The value of an end bit of a full code is "0" and one bit of value "0" and more is/are inserted between two bits of value "1" in the code. Furthermore, the number of the bit of value "0" are restricted to eight and below. The number of the sequence of bit of value "0" at both the end parts of the code are restricted to 4 and below. Therefore, one bit of value "0" and over or eight bits of value "0" and below are contained between two bits of value "1" in the code sequence. The above-mentioned code is assigned to digital data as follows:

d=1

k=8

At first, a CDS (code word digital sum) of the full code are calcurated, and respective code wherein the CDS is equal to zero (CDS = 0) are allotted uniquely to each of the digital data. Furthermore, for the cases that CDS ≠ 0 respective "pairs" of the codes of

CDS = +2 and CDS = −4,

CDS = −2 and CDS = +4,

CDS = +2 and CDS = −6 and

CDS = −2 and CDS = +6

are allotted to the digital data. In the above-mentioned pair of the code, a code having small CDS in value, for example, the code of CDS = ±2 is grouped in a "group A". The codes of CDS = ±4 and CDS = ±6 is grouped in a "group B". The code of CDS = 0 belongs to both the group A and the group B.

A selecting method of the code corresponding to the digital data is elucidated as follows: The encoding of a digital data is processed referring to a value of DSV at an end of the preceding code of the present code corresponding to the digital data and a polarity wherein H level of the end bit of the above-mentioned code is assigned to the positive polarity and L level of that is assigned to the negative polarity when an NRZI encoding is applied to the digital data.

The change of the DSV value and the polarity are shown in FIG.2. The polarity of the wave form of NRZI encoding alternatives at the bit of value "1" of the code sequence. The relation between CDS and DSV of the code is shown in FIG.12. As shown in FIG.12(a), the code wherein the value of CDS is positive increases DSV when the polarity of the starting point of the code is negative, and decreases DSV when the polarity of the starting point of the code is positive. As shown in FIG.12(b), the code wherein the value of CDS is negative decreases DSV when the polarity of the starting point of the code is negative, and increases DSV when the polarity of the starting point of code is positive. As shown in FIG.12(c), the code wherein the value of CDS is "0" maintains DSV at a constant value independent of the polarity of the starting point of the code.

The manner of selecting the code is shown in Table 2.

Table 2

DSV at the end point of the preceding code	Polarity at the end point of the preceding code	Usable code	Changing of DSV	
Positive	Positive	Code wherein CDS is positive or zero	Decrease or constant	A
	Negative	Code wherein CDS is negative or zero	Decrease or constant	B
Zero	Positive	Code of group A	+2 or 0 or +2	C
	Nagative			
Negative	Positive	Code wherein CDS is negative or zero	Increase or constant	D
	Nagative	Code wherein CDS is positive or zero	Increase or constant	E

The code is selected as it goes to negative value when the value of DSV is positive, and it goes to positive value when the value of DSV is negative. Therefore, the change of value of DSV is restricted in a constant range wherein value "0" is on the center of the constant range.

As shown in column A of Table 2, when the value of DSV at the end point of the code which corresponds to a preceding digital data of the present digital data is positive, the polarity is also positive. The code wherein CDS is positive or zero is selected from the group A and the group B corresponding to the digital data, and is allotted to the digital data.

As shown in the column B of the Table 2, when the value of DSV at the end point of the code which corresponds to a precedidng digital data is positive, and the polarity is negative. The code wherein CDS is negative or zero is selected from the group A and the group B corresponding to the digital data, and is allotted to the digital data.

As shown in the column D of the Table 2, when the value of DSV at the end point of the code which corresponds to a preceding data of the present digital data is negative and the polarity is positive, the code wherein CDS is negative or zero is selected from the

group A and the group B corresponding to the digital data, and is allotted to the digital data.

As shown in the column E of the Table 2 when the value of DSV at the end point of the code which corresponds to a preceding digital data of the present digital data is negative and the polarity is negative, the code wherein CDS is positive or zero is selected from the group A and the group B corresponding to the digital data, and is allotted to the digital data.

When the value of DSV at the end point of the code which corresponds to the preceding digital data is negative, a DSV-flag correspond to the bit with value "1". When the value of DSV on the above-mentioned condition is positive, the DSV-flag correspond to the bit with value "0". When the polarity on the above-mentioned condition is negative, a polarity flag correspond to the bit of value "1", and when the polarity on the above-mentioned condition is positive, the polarity signal correspond to the bit of value "0". When the exclusive logical sum of the DSV-flag and the polarity signal is "1", the encoding code wherein CDS is negative or zero is allotted to the digital data. As shown in the column C of the Table 2, when the value of DSV at the end point of the code which correspond to the preceding digital data of the present digital data is zero, the code of the group A wherein the absolute

value of CDS is small is allotted to the digital data independent of the polarity, and variance of DSV is ±2 or zero. As a result, the value of DSV of the code sequence is limited to a constant range.

In the present embodiment, the absolute value of DSV is equal to or within ±9, and is "0", "±2" or "±4" at the end part of the respective codes.

An example of encoding circuit for encoding algorithm in accordance with the present invention is shown in FIG.1, and the timing chart in the operation of the encoding circuit is shown in FIG.3.

In FIG.1, parallel 8-bit digital data are inputted to a ROM 13 and a ROM 14 through an input terminal 1. A reset signal is applied to a five bit latch 17 through a reset input terminal 3. A latch clock is inputted to the latch 17 through a latch clock input terminal 5. A code is issued from a code output terminal 7. A shift/load switching signal is applied to a 14-bit shift register 15 through a shift/load switching signal input terminal 9. A code readout clock is inputted to the shift register through a code readout clock terminal 11. The output of the code output ROM 13 is applied to the shift register 15. A ROM 14 issues CDS signals and polarity signals. A 4-bit full-adder 16 is connected between the ROM 14 and the latch 17. A distinction circuit 18 is formed by

three OR gates and distincts the value of DSV at the end point of a code wherein a preceding digital data of the present digital data are encoded. A selection circuit 19 is formed by an exclusive OR gate.

The encoding operation is shown by the timing chart of FIG.3. A low level reset signal for an initial setting is inputted to the latch 17 at a time as shown in FIG.3(a), and the output level of the latch 17 is set to "0". As a result, a distinction signal from the distinction circuit 18, a selection signal and a polarity signal are set to "0". Parallel 8-bit digital data are inputted to the ROM 13 and the ROM 14 in order of d_1, d_1, d_2, d_3, ... through the digital data input terminal 1. Furthermore, the distinction signal and the selection signal are inputted to the ROM 13. The distinction signal, the selection signal and the polarity signal are inputted to the ROM 14. The distinction signal is an output signal wherein a value of DSV at the end point of preceding digital data of the present digital data is discriminated by the distinction circuit 18. When DSV is "0", the output signal is "0". When DSV is not "0", the output signal is "1". The selection signal is an output signal of the selection circuit 19 and is equal to an exclusive logical sum of the polarity signal (A positive signal is "0", and a negative signal is "1".) and to a DSV-

flag 23 (A positive flag is shown by "0" and negative flag is shown by "1".) which shows the polarity of DSV.

The ROM 13 processes the 8-bit digital data, the distiction signal and the selection signal, and then outputs a 14-bit code to the shift register 15 according to conditions as shown in the Table 2. The selection of the code, as shown in Table 2, when the distinction signal is "0", the code of the group A wherein an absolute value of CDS is smaller one of two codes corresponding to the 8-bit digital data which are encoded is selected. When the distinction signal is "1" and the selection signal is "0", namely, in Table 2, when DSV at the end point of the code wherein preceding digital data of the present digital data are encoded is positive and the polarity is also positive, and furthermore, when DSV is negative and the polarity is negative, the code wherein CDS is positive or zero is selected from the above-mentioned two codes. When the selection signal is "1", namely in Table 2, when DSV is positive and the polarity is negative, furthermore when the DSV is negative, and the polarity is positive, the code wherein CDS is negative or zero is selected from the above-mentioned two codes.

A shift/load switching signal is inputted to the shift register 15 through the shift/load switching signal input terminal 9, and the code which is output

from the ROM 13 is parallelly inputted to the shift register 15 when the shift/load switching signal turns to low level as shown in FIG.3. Code readout clocks 12 are inputted at a timing as shown in FIG.3 from the clock input terminal 11, and the above-mentioned code is serially read. The code which is converted to the serial code is issued from the output terminal 7 in order of D_1 , D_2 , D_3 , ... at a timing as shown in FIG.3. In FIG.3, the time period is enlarged in the abscissa which is drawn by dotted lines. The code which is output by the ROM 13 is decided in the ROM 14 in view of the input 8-bit digital data, the distinction signal and the selection signal.

A variation of DSV which is caused by CDS of the code which is issued from the ROM 14 is output in accordance with the polarity signal. When the variation of DSV is zero, the variation is represented by the binary "0000", and similarly when the variation of DSV are +2, +4, +6, -2, -4 and -6, the respective variations are represented by the binaries "0010", "0100", "0110", "1110", "1100" and "1010", respectively. These variations are inputted to the 4-bit full adder 16. When the number of the bit "1" of the above-mentioned decided code is odd, the ROM 14 reverses the polarity of the input polarity signal and output to the latch 17. When the number of the bit "1"

is even, the ROM 14 does not reverse the polarity of the input polarity signal and output to the latch 17.

In the 4-bit full adder 16, the value of DSV at the end point of the code sequence wherein the preceding digital data of the present digital data are encoded and is issued from the latch 17, and the variation of DSV in accordance with the code of the present digital data are added, and the value of DSV at the end point of the code wherein the above-mentioned present digital data is encoded is output to the latch 17. In the latch 17, the inputted new DSV and the polarity signal are held by a rise of latch clock 6 which is inputted from the latch clock input terminal 5 at a timing as shown in FIG.3.

The value of DSV at the end point of the code wherein the above-mentioned present digital data is encoded and is output from the latch 17 is applied to the distinction circuit 18, and is used for encoding next digital data to the present digital data.

The polarity signal is inputted to the selection circuit 19 and to the ROM 14, and is used for encoding next digital data. The above-mentioned process is repeated and the encoding is proceeded. Secondly, an NRZI coding is applied to the code sequence wherein the digital data sequence is encoded in an NRZI coder sequence, and the NRZI code is

recorded on the magnetic recording medium through a rotary transformer and a magnetic head of the recording part.

In the reproduction process, the NRZI code sequence is reproduced throught the common rotary transformer and a magnetic head of the reproducing part, and the NRZI decoding is processed in the NRZI decoder, and furthermore, a decoding of 8-14 code is processed.

An embodiment of a decoding circuit in accordance with the present invention is shown in FIG.4. The code is inputted to a 14-bit shift register 52 through an input terminal 30. Clock signals are inputted through an input terminal 32. Output signals of the shift register 52 are applied to a 14-bit latch 53. Latch clock signals are inputted through a latch clock input terminal 34. Output signals of the latch 53 are inputted to a ROM 54 for decoding. Decoded digital data are issued parallelly from output terminals 36--43. A timing chart showing the operation of the decoding circuit is shown in FIG.5. The reproduced code are inputted to the shift register 52 sequentially in the order, D_0 , D_1 , D_2 , ... The clock signals are inputted to the shift register 52 through the terminal 32 at a timing as shown in FIG.5. In FIG.5, a range along an abscissa which is shown

enlarged by a dotted line of the clock.

The code sequence which is sequentially inputted from the terminal 33 is shifted one by one of bit synchronizing the clock 33 and is issued to the latch 53 in the shift register 52. The reproduced code sequence is separated to every code which is formed by 14-bit, and is issued to the ROM 54 in the latch 53. For this object, the latch clock 35 which is formed by detecting the below-mentioned frame synchronizing signal is inputted in the latch 53 through the terminal 34 at a timing as shown in FIG.5, and is latched by the rise of the clock 35. The 14-bit code which is issued from the latch 53 is inputted to the ROM 54 as an address, and 8-bit digital data 44--51 corresponding to the above-mentioned 14-bit code are output. The decoded digital data are output parallelly from the output terminals 36--43.

As mentioned above, since the number of bit "0" which is inserted between two bit "1" is restricted to from one to eight, when the code is recorded on the magnetic recording medium.

The minimum magnetization reversal interval becomes 1.14T (T is a periodic time of the digital data), the maximum magnetization reversal interval becomes 5.14T, and DR becomes 1.14, and the high density recording is realized. The encoded digital

data of the respective pairs of CDS = +2 and CDS = -4, CDS = -2 and CDS = +4, CDS = +2 and CDS = -6 and CDS = -2 and CDS = +6 are allotted to the digital data, and when DSV is not zero, DSV can be restricted to ±9 and below, and DC component decreased. Correspondence between the digital data and the code as shown in Table 1 is changeable. If two codes wherein polarities and absolute values of CDS are different from each other are combined, the combinations of the codes are freely selected.

The frame synchronizing signal is elucidated as follows: The value of the end bit of the code is "0" and the bit "0" of one and over are contained between two bits "1", and the maximum number of the successive bits "0" are limited to eight in the each 14-bit code. Furthermore, the maximum number of the successive bit "0" are limited to four at the head part and the tail part of the code. Furthermore, the code which consists of 14-bit and wherein the bits "0" of three and over continue at the head part or the tail part is excepted from the code. Moreover, the code wherein the bits "0" of seven and over follow to the above-mentioned successive three bit "0" and a bit "1" is inserted between the two groups of bit "0" is also excepted from the code. Therefore, the pattern of "10000000" appears at the successive part of the code,

however, the successive patterns of "10000000" do not appear at the front and the rear of the above-mentioned pattern. Therefore, the pattern of "1000000010000000" does not appear in the code sequence. The bit "10" is added to the end of the pattern in order to meet to the above-mentioned restriction of succession of the bit "0". Similarly, the bit "10" is added to the head of the pattern in order to meet to the restriction of continuation of the bit "0" and to make CDS of the frame synchronizing signal to zero.

The following 28-bits of "XXXXXXXXXX100000001000000010" are used for a frame synchronizing signal. (The part which is shown by "X" represents an optionally decided ten bits of "10" wherein the restriction of succession of the bit "0" is satisfied and CDS of the synchronizing signal of 28-bit become "0".)

In FIG.6, the block diagram of a signal processing circuit including an addition part of the frame synchronizing signal and a detection part in accordance with the present invention is shown. The digital data are inputted to a frame forming part 62 through a digital data input terminal 60. The output of the frame forming part 62 is applied to an encoder 63. The output of the encoder 63 is applied to a frame synchronizing signal addition part 64. The output of

the frame synchronizing signal addition part 64 is applied to an NRZI encoder 65. The output of the NRZI encoder 65 is recorded on a recording medium through a recording part 66.

In a reproduction process, the recorded signals are detected by a reproduction part 67, and are decoded by an NRZI decoder 68. The output of the NRZI decoder is inputted to a frame synchronizing signal detection part 69 and a shift register 70. The output of the shift register 70 is applied to a decoder 71. An encoded digital data separation signal is output from the frame synchronizing signal detection part 69 and is inputted to the shift register 70. The output of the decoder 71 is applied to a shift register 72 and is issued from a digital data output terminal 73. As shown in FIG.7, a dummy synchronizing signal, an address, an address error detecting code and an error correction code are added to a digital data, thereby to form a frame in the frame forming part 62. The frame is output to the encoder 63. The frame is encoded in accordance with the above-mentioned 8-14 encode algorithm by the encoder 63, and the encoded frame signal is applied to the frame synchronizing signal addition circuit 64. In the frame synchronizing signal addition circuit 64, the dummy synchronizing signal which

normal synchronizing signal of "XXXXXXXXXX100000001000000010". The frame synchronizing signal addition circuit is shown in FIG.8. A switching signal and the code sequence are inputted to a switching circuit 86 in accordance with the timing as shown in FIG.9 through a switching signal input terminal 80 and the code sequence input terminal 81, respectively. The code sequence wherein the frame synchronizing signal is replaced is output from the code output terminal 85. A shift/load signal and a readout clock are inputted to a shift register 87 in accordance with the timing as shown in FIG.9 through a shift/load signal input terminal 82 and a readout clock input terminal 83, respectively. The shift register 87 is a 28-bit parallel input and serial output shift register. The shift register 87 reads a frame synchronizing signal in accordance with the shift/load signal 82 and outputs the frame synchronizing signal to the switching circuit 86 synchronizing readout clock 83. In switching circuit, the dummy synchronizing signal of the code sequence is replaced by the frame synchronizing signal and the code is output.

The frame synchronizing signal detection circuit 69 is shown in FIG.10. Reproduced code sequence is inputted to a 16-bit shift register 91 in the frame synchronizing signal detection circuit 69.

The above-mentioned reproduced code sequence is shifted one by one of bits by the clock signal 94 in the shift register 91. The output of the shift register 91 is inputted to a comparator 92 and is compared with a 16-bit pattern "1000000010000000" which does not appear in the code sequence of the frame synchronizing signal which consist of 28-bit, and the synchronizing signal of each frame is detected. When the output of the shift register 91 agrees with the 16-bit pattern, a detecting signal 93 is output from the comparator 92 and is applied to a counter 95. The counter 95 is loaded with a predetermined value by the detecting signal 93, and is operated as a counter wherein the figure is taken up at fourteen. As a result, a code dividing signal 96 for dividing the reproduced code sequence into respective codes is output.

In FIG.6, the shift register 70 divides the reproduced code sequence which is inputted serially into the codes and applied to the decoder 71. In the decoder 71, the 8-bit digital data corresponding to the inputted code is output to the shift register 72. The inputted 8-bit digital data is output serially from the digital data output terminal 73. As mentioned above, the frame synchronizing signal including the 16-bit pattern "1000000010000000" which does not appear in the code sequence, when 8-14 encoding is adopted, is

recorded. Hence, the frame synchronizing signal can be detected precisely by a simple circuit.

WHAT IS CLAIMED IS

1. Digital data recording and reproducing method comprising:

dividing digital data to every 8-bit digital data,

selecting one of two codes wherein an absolute value of digital sum variation of NRZI coded wave form wherein a code sequence of said digital data is encoded to NRZI code decreases,

wherein number of bit "0" inserted between two bits "1" in a code sequence is restricted to a number from one to eight and below, when said 8-bit digital data is allotted to one or two codes.

2. Digital data recording and reproducing method in accordance with claim 1, wherein

codeword digital sum of respective codes are caluculated, and

a code wherein said codeword digital sum is zero is made to correspond to an 8-bit digital data and a pair of a code wherein codeword digital sum is not zero and another code wherein polarity of codeword digital sum and an absolute value of codeword digital sum are different from said code is made to correspond to said 8-bit digital data.

3. Digital data recording and reproducing apparatus comprising:

means for producing NRZI coding of a code sequence wherein an 8-bit digital data is sequentially coded,

means for issuing a control signal which selects 14-bit code wherein an absolute value of digital sum variation of a wave form of said NRZI code decreases, and

means for issuing a 14-bit code corresponding to said 8-bit digital data by input of said control signal.

4. Digital data recording and reproducing apparatus in accordance with claim 3, wherein

means to generate said control signal comprises:

means for calculating a variation of digital sum variation which is changed by said 14-bit code,

means for adding said variation of digital sum variation and a value of digital sum variation before said variation arise,

means for memorizing the value of digital sum variation which is calculated by addition process,

means for discriminating a value of digital sum variation,

means for realizing a polarity at an end point of said 14-bit code,

means for memorizing said polarity, and

means for deciding issue either of a code wherein CDS is positive or zero or a code wherein CDS is negative or zero.

5. Digital data recording and reproducing method in accordance with claim 2, wherein

a bit sequence which never arise in a code sequence wherein a digital data sequence is encoded is used as a frame synchronizing signal.

6. Digital data recording and reproducing method in accordance with claim 5, wherein

an N-bit sequence ($N \geq 16$) including a pattern "1000000010000000" which does not coincide to an optional continuous 16-bit code which is extracted from a code sequence wherein a digital data sequence is encoded is recorded as a frame synchronizing signal.

FIG.1

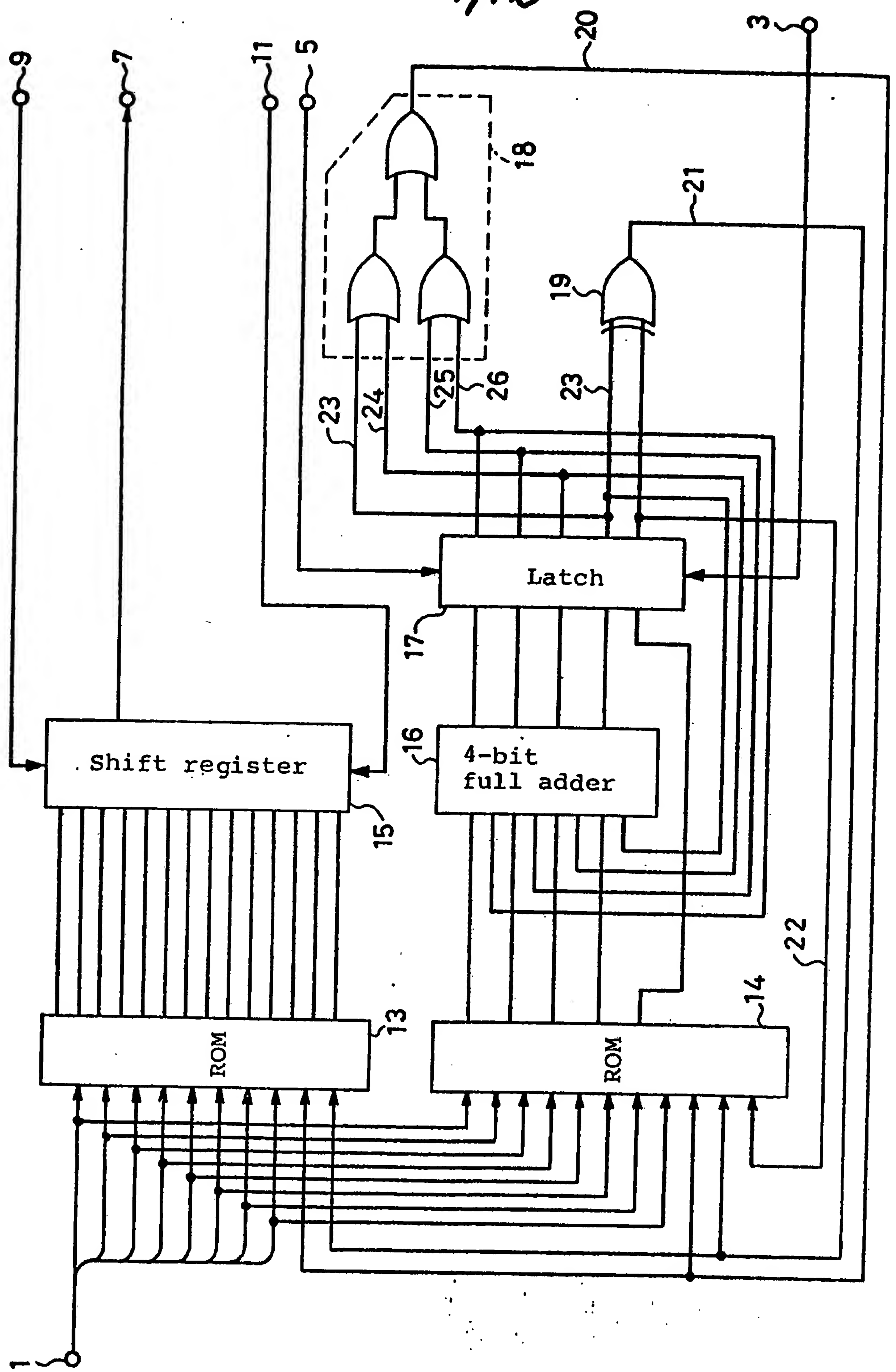
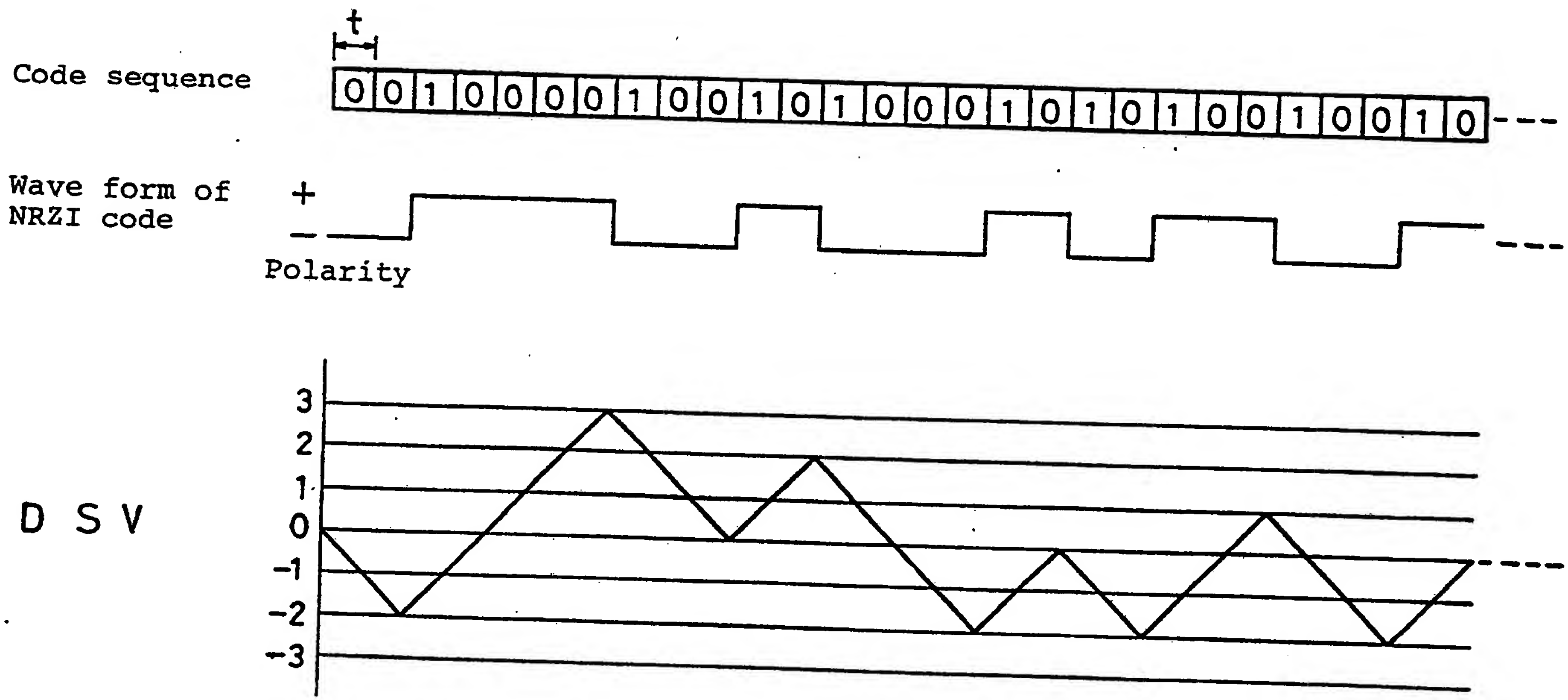

Shift register
Latch
4-bit
full adder
ROM
ROM
1
3
5
7
9
11
13
14
15
16
17
18
19
20
21
22
23
24
25
26
23

FIG. 2


t
Code sequence
0 0 1 0 0 0 0 1 0 0 1 0 1 0 0 0 1 0 1 0 1 0 0 1 0 0 1 0
Wave form of NRZI code
+
−
Polarity
DSV
3
2
1
0
−1
−2
−3

F I G. 3

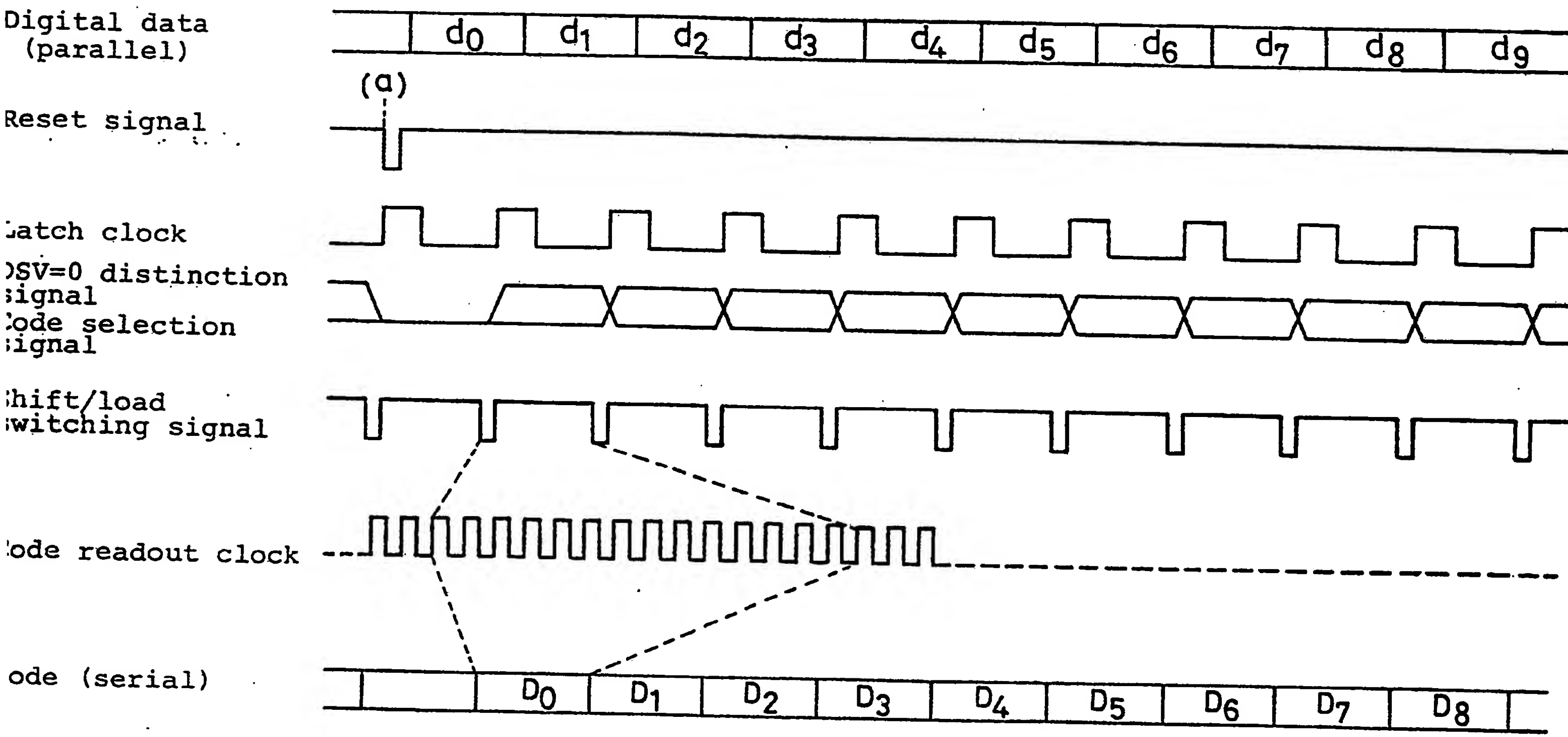
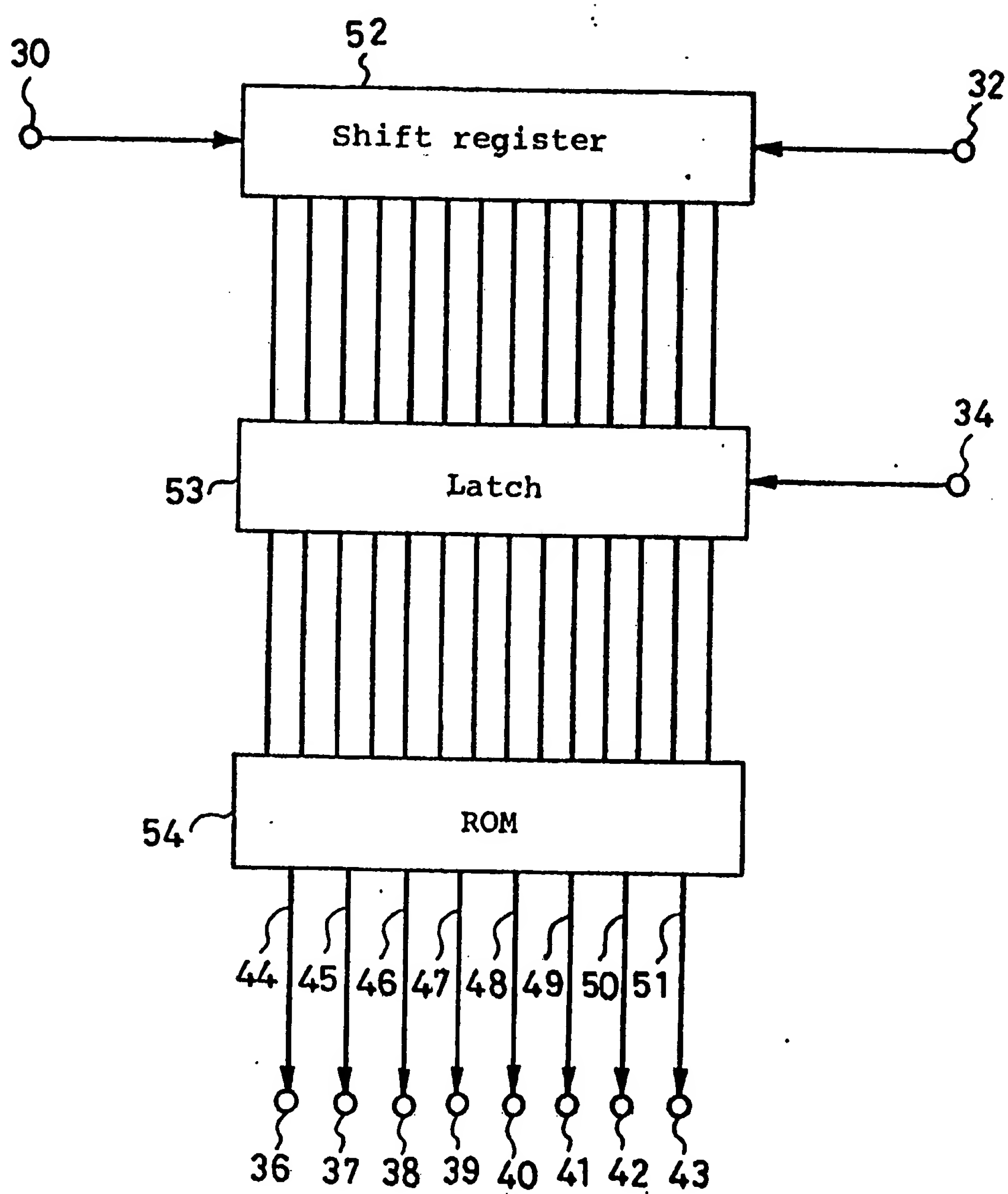

Digital data (parallel)
d0 d1 d2 d3 d4 d5 d6 d7 d8 d9
(a)
Reset signal
Latch clock
DSV=0 distinction signal
Code selection signal
Shift/load switching signal
Code readout clock
Code (serial)
D0 D1 D2 D3 D4 D5 D6 D7 D8

FIG. 4



30
52
Shift register
32
34
53
Latch
54
ROM
44
45
46
47
48
49
50
51
36
37
38
39
40
41
42
43

FIG.5

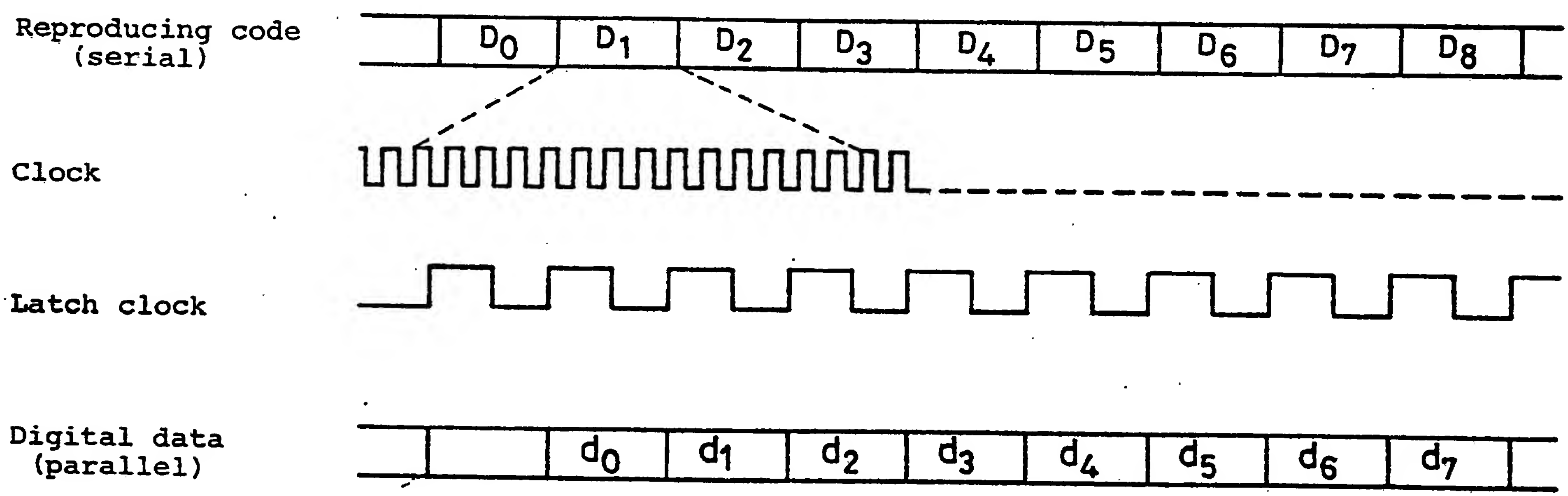

Reproducing code (serial)
Clock
Latch clock
Digital data (parallel)
D0 D1 D2 D3 D4 D5 D6 D7 D8
d0 d1 d2 d3 d4 d5 d6 d7

FIG.6(a)

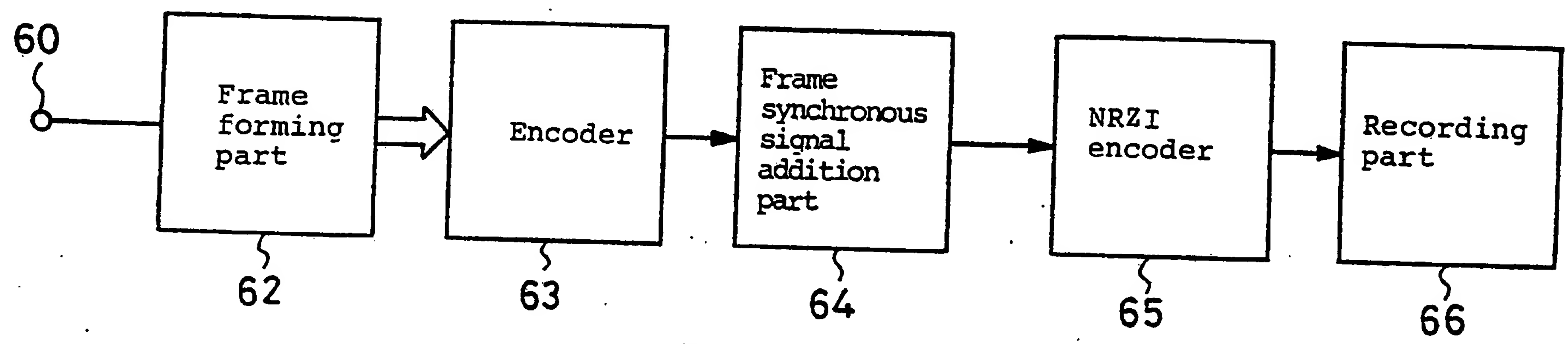

60
Frame forming part
62
Encoder
63
Frame synchronous signal addition part
64
NRZI encoder
65
Recording part
66

FIG.6(b)

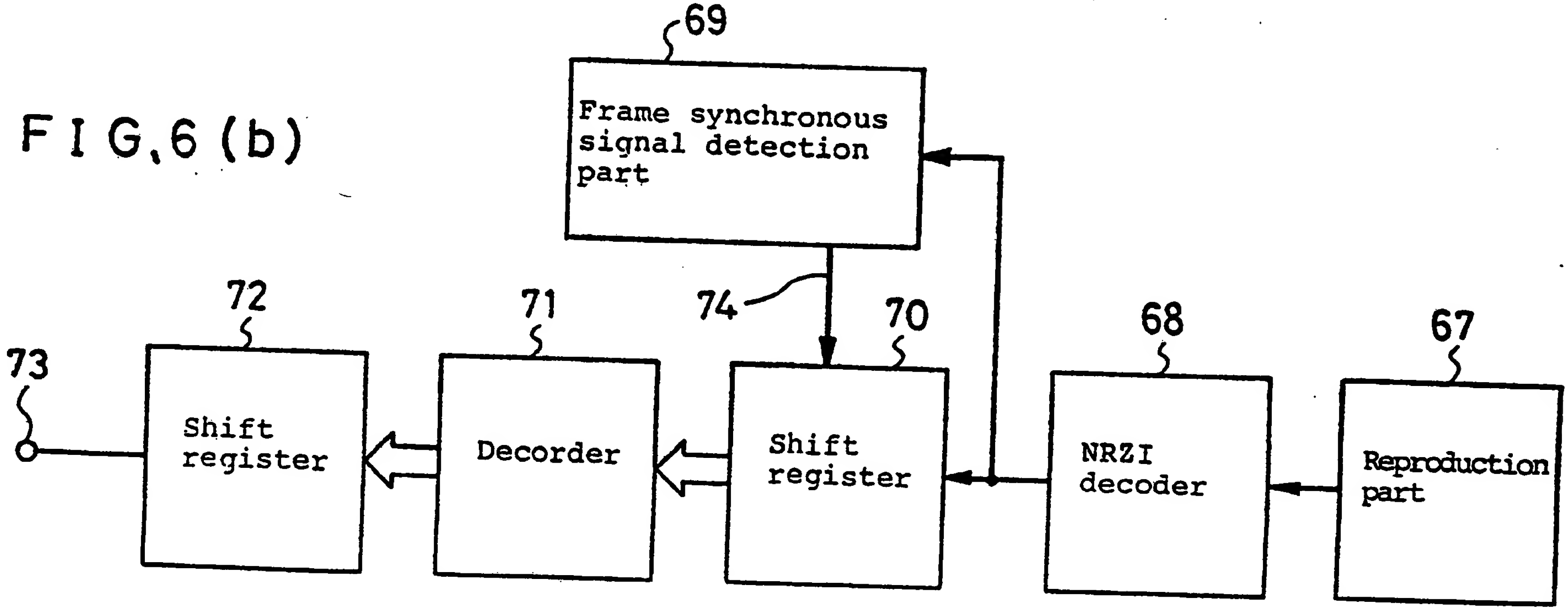
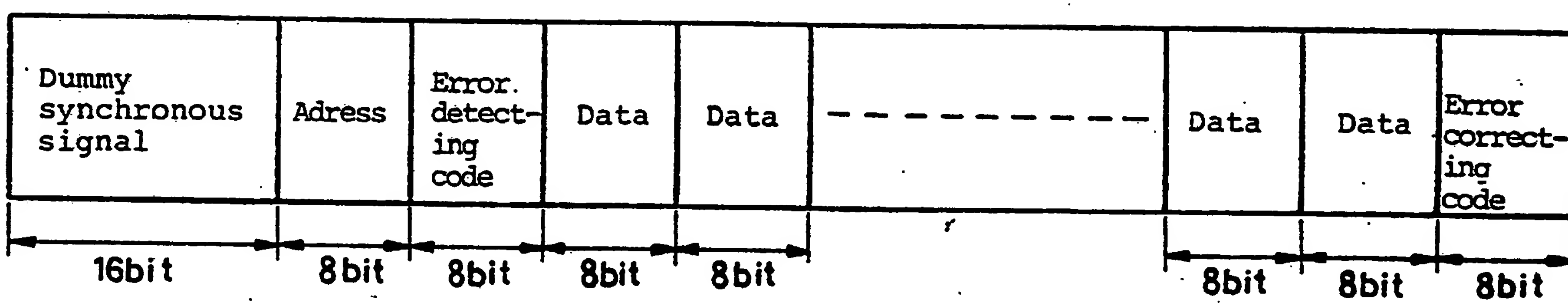
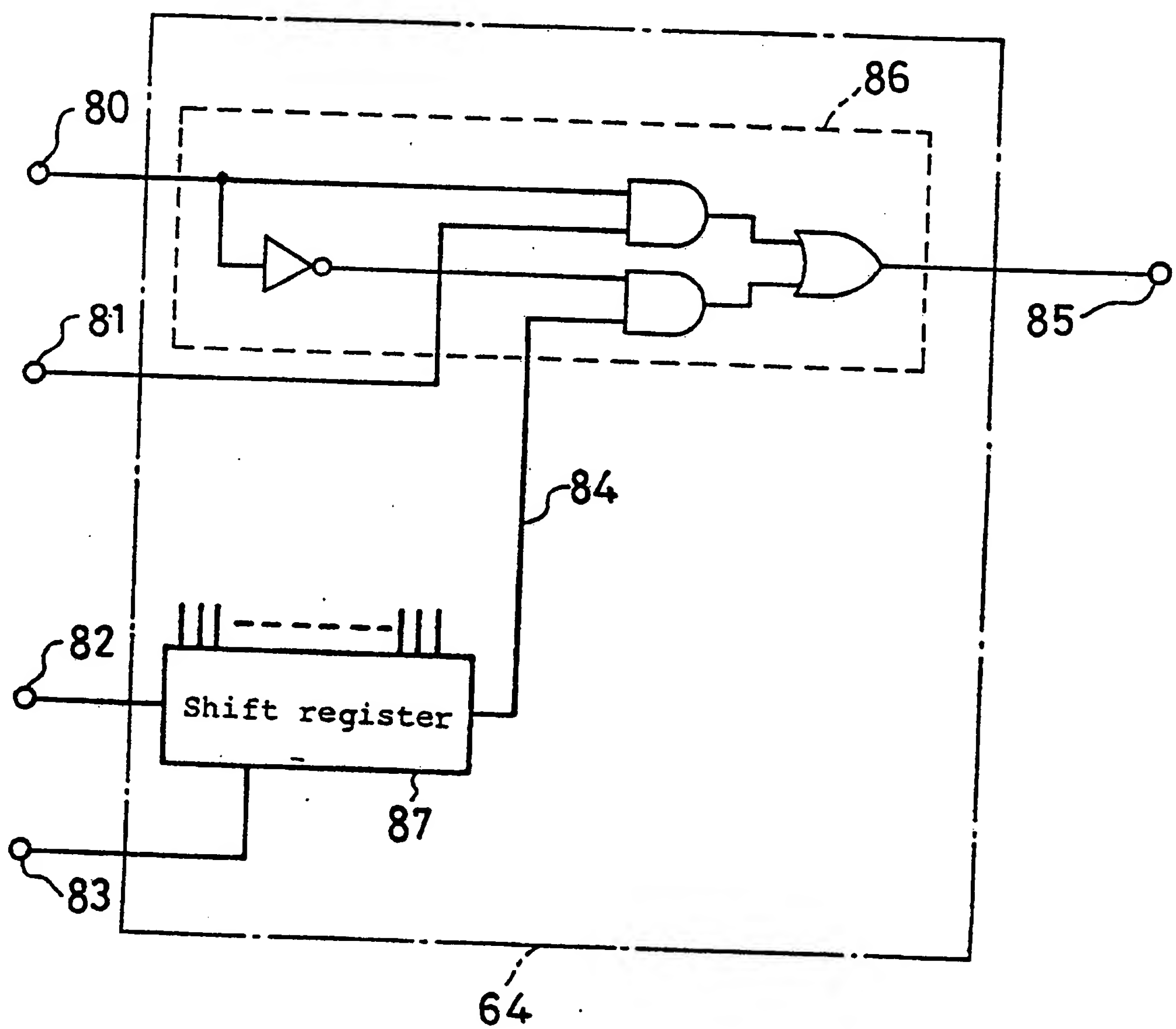

69
Frame synchronous signal detection part
74
70
Shift register
68
NRZI decoder
67
Reproduction part
71
Decorder
72
Shift register
73

FIG.7



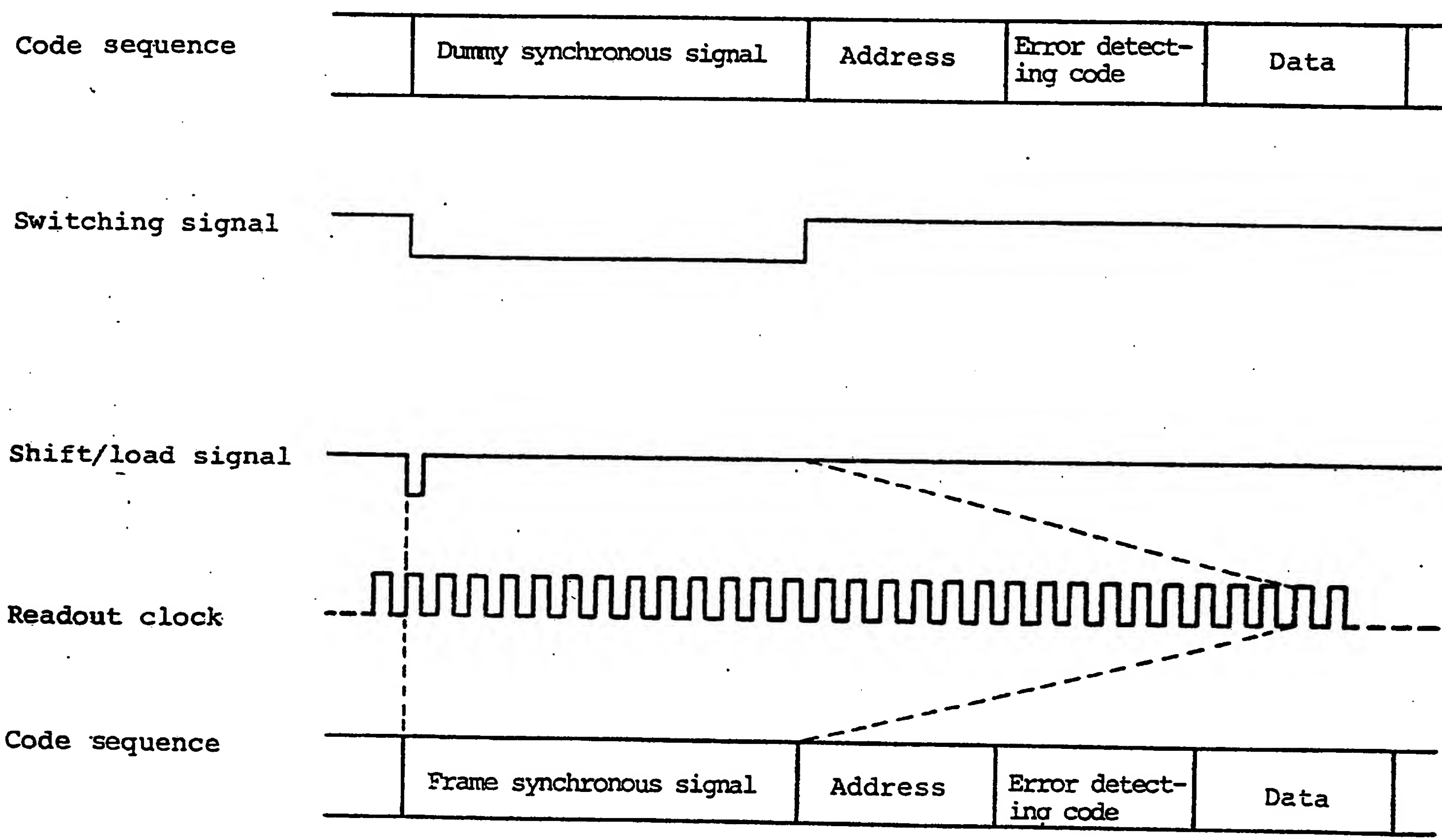
Dummy synchronous signal
Adress
Error. detecting code
Data
Data
Data
Data
Error correcting code
16bit
8bit
8bit
8bit
8bit
8bit
8bit
8bit

FIG. 8



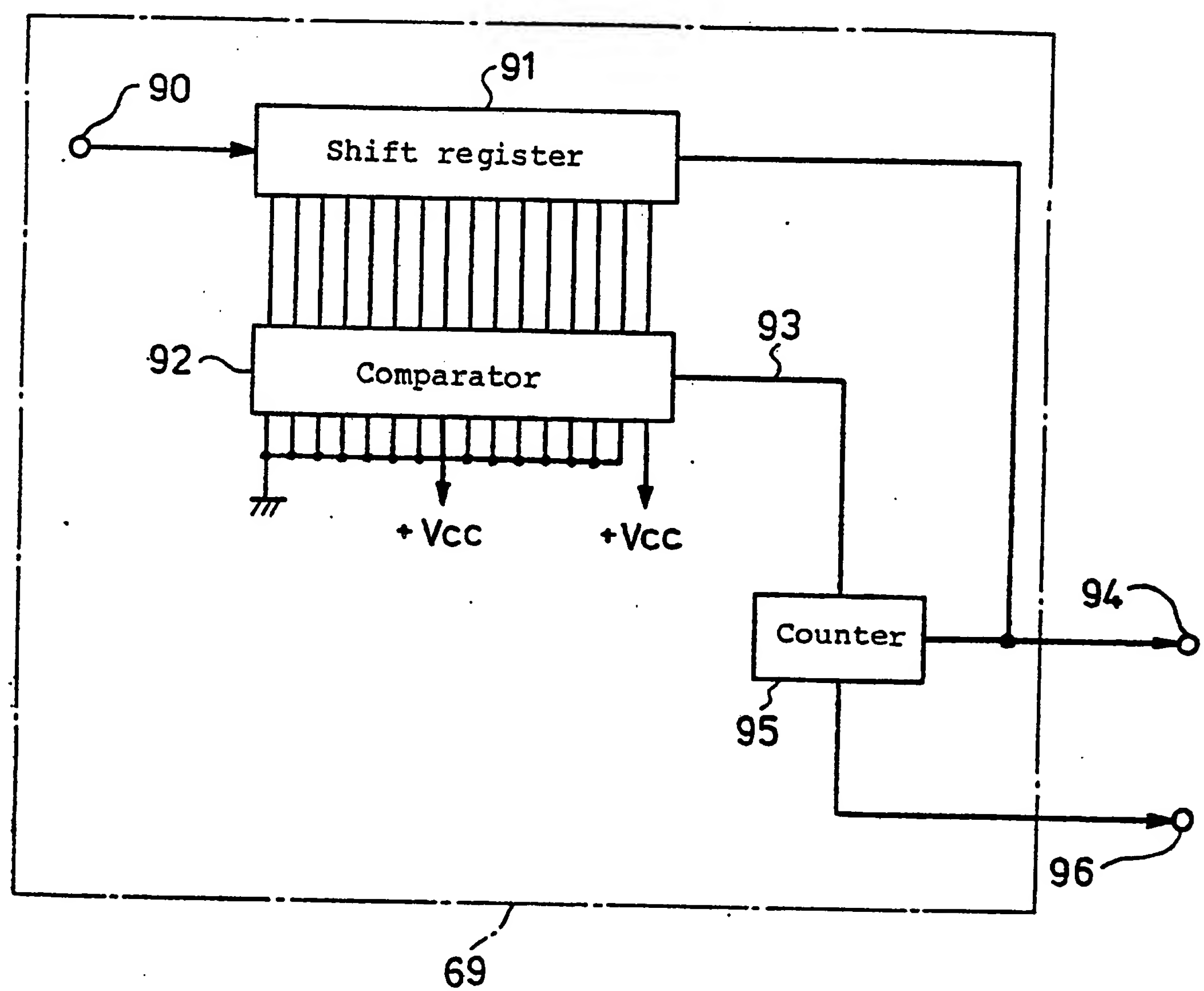
9/12

F I G. 9



Code sequence
Dummy synchronous signal
Address
Error detect-ing code
Data
Switching signal
Shift/load signal
Readout clock
Code sequence
Frame synchronous signal
Address
Error detect-ing code
Data

FIG. 10



90
91
Shift register
92
Comparator
93
+Vcc
+Vcc
Counter
95
94
96
69

FIG.11 (a)

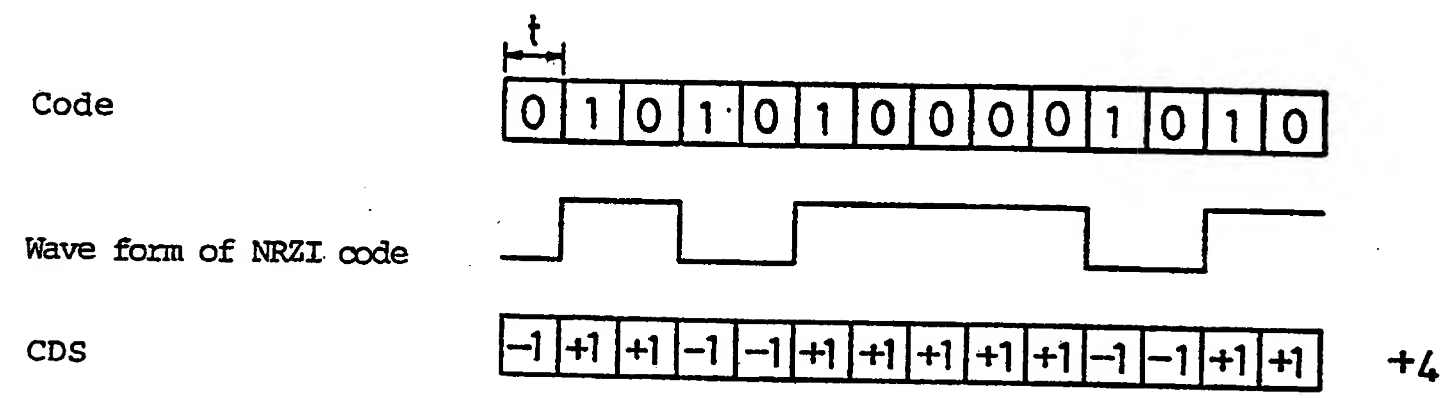


FIG.11 (b)

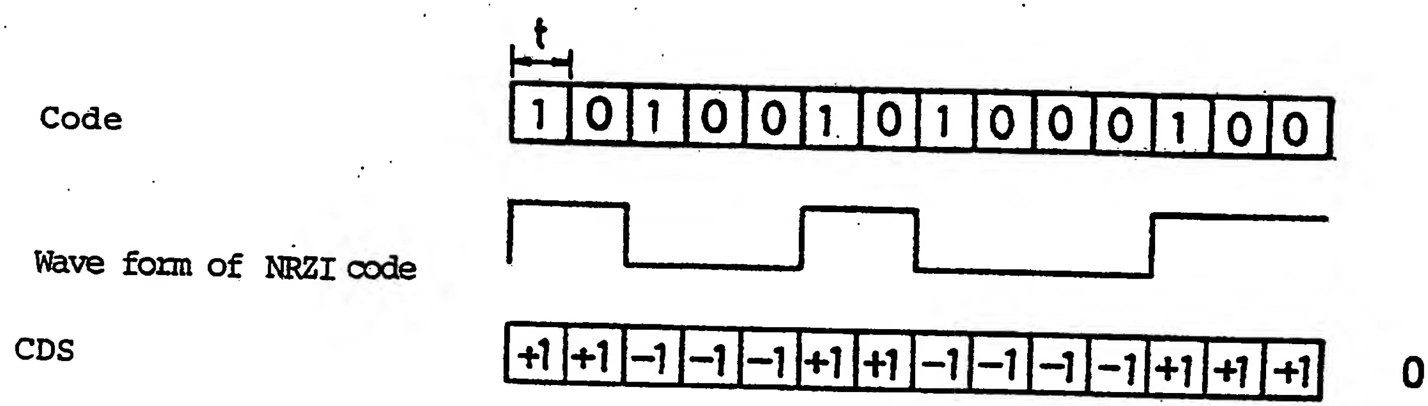


FIG. 12 (a)

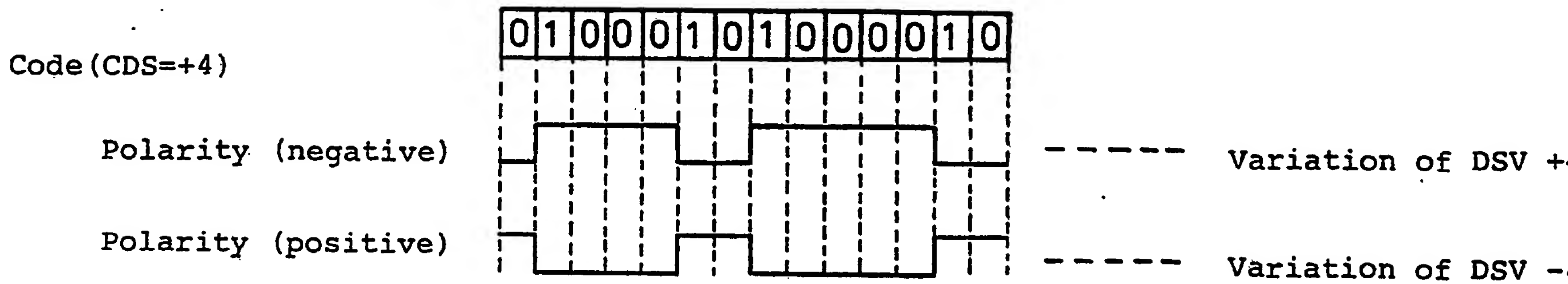


FIG. 12 (b)

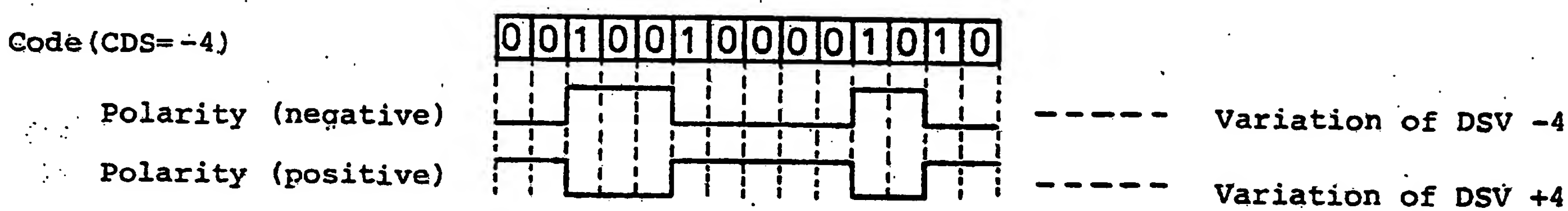


FIG. 12 (c)